IN THE CLAIMS

1-35. (Canceled)

36. (Currently Amended) A field emitter array, comprising:

a number of cathode emitter tips formed in rows along a substrate;

a single gate insulator having a thickness that is thinner than a height of the number of cathode emitter tips, formed along the substrate and surrounding the cathode emitter tips;

a number of gate lines formed on the gate insulator; and

a number of anodes formed in columns orthogonal to and opposing the rows of cathodes, the field emitter array formed by a method comprising:

forming a number of cathode emitter tips in cathode regions of the substrate;

forming a single gate insulator layer on the emitter tips and the substrate, wherein forming the single gate insulator layer includes ion etching the insulator layer such that the insulator layer is formed thinner around the emitter tips than in an isolation region of the substrate;

forming a number of gate lines on the gate insulator layer; and

forming a number of anodes opposite the emitter tips, and

wherein a distance separating the number of cathode emitter tips from the number of gates lines is significantly thinner than a separation distance separating the number of gate lines and the substrate.

37. (Previously Presented) The field emitter array of claim 36, wherein the number of gate lines and the number of cathode emitter tips are formed using a self-aligned technique.

38. (Previously Presented) The field emitter array of claim 36, wherein the number of cathode emitter tips include polysilicon cones.

39. (Previously Presented) The field emitter array of claim 38, wherein the number of cathode emitter tips include metal silicides on the polysilicon cones.

40. (Original) The field emitter array of claim 36, wherein the substrate includes glass.

41. (Original) The field emitter array of claim 36, wherein the number of gate lines include refractory metals.

42. (Original) The field emitter array of claim 36, wherein the number of gate lines include doped polysilicon.

43. (Previously Presented) A flat panel display, comprising:

a field emitter array formed on a glass substrate, wherein the field emitter array includes:

a number of cathode emitter tips formed in rows along the substrate;

a single gate insulator formed along the substrate and surrounding the cathode emitter tips;

a number of gate lines formed on the single gate insulator; and

a number of anodes formed in columns orthogonal to and opposing the rows of cathodes, wherein the anodes include multiple phosphors, and wherein the intersection of the rows and columns form pixels, the field emitter array formed by a method comprising:

forming a number of cathode emitter tips in cathode regions of the substrate;

forming a single gate insulator layer on the emitter tips and the substrate, wherein forming the single gate insulator layer includes ion etching the insulator layer such that the insulator layer is formed thinner around the emitter tips than in an isolation region of the substrate;

forming a number of gate lines on the gate insulator layer; and

forming a number of anodes opposite the emitter tips;

wherein a distance separating the number of cathode emitter tips from the number of gates lines is significantly thinner than a separation distance separating the number of gate lines and the substrate;

a row decoder and a column decoder each coupled to the field emitter array in order to selectively access the pixels; and

a processor adapted to receiving input signals and providing the input signals to the row and column decoders.

44. (Previously Presented) The flat panel display of claim 43, wherein the number of gate lines and the number of cathode emitter tips are formed using a self-aligned technique.

45. (Previously Presented) The flat panel display of claim 43, wherein the number of cathode emitter tips include metal silicides on polysilicon cones.

46. (Original) The flat panel display of claim 43, wherein the number of gate lines include refractory metals.

47. (Currently Amended) A field emitter array, comprising:

a number of cathode emitter tips in rows along a substrate;

a single gate insulator located along the substrate and surrounding the cathode emitter tips, the single gate insulator having a gate line region thickness that is thinner than a height of the number of cathode emitter tips;

a number of gate lines coupled to the gate insulator, wherein a gate line to cathode emitter tip distance between a portion of the gate line and the cathode emitter tip is substantially thinner than the gate line region thickness; and

a number of anodes located in columns orthogonal to and opposing the rows of cathode emitter tips.

48. (Previously Presented) The field emitter array of claim 47, wherein the number of cathode emitter tips include polysilicon cones.

49. (Previously Presented) The field emitter array of claim 47, wherein the number of gate lines include refractory metals.

50. (Previously Presented) The field emitter array of claim 47, wherein the number of gate lines include doped polysilicon.

51. (Currently Amended) A field emitter array, comprising:

a number of cathode emitter tips in rows along a substrate;

a single gate insulator located along the substrate and surrounding the cathode emitter tips, the single gate insulator having a gate line region thickness that is thinner than a height of the number of cathode emitter tips;

a number of gate lines coupled to the gate insulator, wherein a gate line to cathode emitter tip distance between a portion of the gate line and the cathode emitter tip is substantially thinner than the gate line region thickness; and

a number of anodes located in columns orthogonal to and opposing the rows of cathode emitter tips;

wherein the number of cathode emitter tips include metal silicides on the polysilicon cones.

52. (Previously Presented) A field emitter array, comprising:

a number of cathode emitter tips in rows along a substrate;

a single gate insulator located along the substrate and surrounding the cathode emitter tips, the single gate insulator having a gate line region thickness;

a number of gate lines coupled to the single gate insulator, wherein a gate line to cathode emitter tip distance between a portion of the gate line and the cathode emitter tip is substantially thinner than the gate line region thickness; and

a number of anodes located in columns orthogonal to and opposing the rows of cathode emitter tips.

53. (Currently Amended) A flat panel display, comprising:

a field emitter array formed on a glass substrate, wherein the field emitter array includes:

a number of cathode emitter tips in rows along a substrate;

a single gate insulator located along the substrate and surrounding the cathode emitter tips , the single gate insulator having a gate line region thickness that is thinner than a height of the number of cathode emitter tips;

a number of gate lines coupled to the gate insulator, wherein a gate line to cathode emitter tip distance between a portion of the gate line and the cathode emitter tip is substantially thinner than the gate line region thickness;

a number of anodes located in columns orthogonal to and opposing the rows of cathode emitter tips; and

a row decoder and a column decoder each coupled to the field emitter array; and

a processor adapted to receiving input signals and providing the input signals to the row and column decoders.

54. (Previously Presented) The flat panel display of claim 53, wherein the number of gate lines and the number of cathode emitter tips are formed using a self-aligned technique.

55. (Previously Presented) The flat panel display of claim 53, wherein the number of cathode emitter tips include metal silicides on polysilicon cones.

56. (Previously Presented) The flat panel display of claim 53, wherein the number of gate lines include refractory metals.

57. (Currently Amended) A flat panel display, comprising:

a field emitter array formed on a glass substrate, wherein the field emitter array includes:

a number of cathode emitter tips in rows along a substrate;

a single gate insulator located along the substrate and surrounding the cathode emitter tips, the single gate insulator having a gate line region thickness that is thinner than a height of the number of cathodes;

a number of gate lines coupled to the gate insulator, wherein a gate line to cathode emitter tip distance between a portion of the gate line and the cathode emitter tip is substantially thinner than the gate line region thickness;

a number of anodes located in columns orthogonal to and opposing the rows of cathode emitter tips, wherein the anodes include multiple phosphors, and wherein the intersection of the rows and columns form pixels; and

a row decoder and a column decoder each coupled to the field emitter array in order to selectively access the pixels; and

a processor adapted to receiving input signals and providing the input signals to the row and column decoders.

58. (Previously Presented) The flat panel display of claim 57, wherein the number of gate lines and the number of cathode emitter tips are formed using a self-aligned technique.

59. (Previously Presented) The flat panel display of claim 57, wherein the number of cathode emitter tips include metal silicides on polysilicon cones.

60. (Previously Presented) The flat panel display of claim 57, wherein the number of gate lines include refractory metals.